## CLAIM AMENDMENTS

Please amend the claims by canceling non-elected claims 63-80, and amending claims 81, 92, 96 and 100, all without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1. - 62. (Previously Cancelled)

63. - 80. (Cancelled)

81. (Currently Amended) In a data storage system having an array of memory cells that individually include an element that stores an electrical charge level that is alterable in response to appropriate voltage conditions being applied to the cell in order to set a variable threshold level thereof into a range that is determinable by reading the cell, the array being organized into blocks of cells that are electrically resetable together to a common threshold level, a method of operation, comprising:

simultaneously electrically resetting the memory cells in a number of said blocks less than all of the blocks in the array,

applying said appropriate voltage conditions in parallel to a plurality of said memory cells within one of the reset blocks in accordance with a chunk of user data, thereby to alter the charge levels on the storage elements of said plurality of memory cells,

determining the threshold level ranges in which individual ones of said plurality of memory cells lie, and

terminating the application of appropriate voltage conditions to individual ones of said plurality of memory cells upon their being determined to have reached desired threshold level ranges while continuing to apply said appropriate voltage conditions to others of said plurality of cells until all of the plurality of cells are determined to have reached their desired threshold level ranges corresponding to said chunk of user data.

82. (Previously presented) The method of claim 81, wherein there are exactly two threshold level ranges.

83. (Withdrawn) The method of claim 81, wherein there are more than two threshold level ranges.

84. (Previously presented) The method of claim 81, wherein the threshold level ranges are separated by exactly one breakpoint threshold level, thereby to provide exactly two non-overlapping threshold level ranges.

85. (Withdrawn) The method of claim 81, wherein the threshold level ranges are separated by more than one breakpoint threshold level, thereby to provide more than two non-overlapping threshold level ranges.

86. (Previously presented) The method of claim 81, additionally comprising, after all of the plurality of cells are determined to have reached their desired threshold level ranges corresponding to said chunk of user data, repeating the applying, determining and terminating operations to additional pluralities of cells within the reset block in order to store additional chunks of user data within the reset block.

87. (Previously presented) The method of claim 81, wherein individual ones of the blocks of cells contain a number of spare cells, and further wherein the spare cells within a particular block are substituted in place of any defective cells within said plurality of cells of said particular block.

88. (Previously presented) The method of claim 81, wherein the plurality of cells are determined to have reached the desired threshold level ranges by comparing the threshold levels of the plurality of cells with the chunk of user data.

89. (Previously presented) The method of claim 81, wherein the chunk of user data is stored in a cache memory prior to being programmed into memory cells within the array.

90. (Previously presented) The method of claim 81, wherein the appropriate voltage conditions are applied to said plurality of memory cells in successive applications of voltage pulses that individually shift the threshold level of the cells to which the voltage pulses are applied less than one half of a total change in threshold voltage that is being made.

91. (Previously presented) The method of any one of claims 81-90, carried out on a single integrated circuit chip.

92. (Currently Amended) The method of either of claims 84 or 85, wherein terminating the application of appropriate voltage conditions to individual ones of the plurality of memory cells occurs upon ~~their~~ the individual cells being determined to have been programmed to within the desired threshold levels by a margin from the breakpoint threshold level.

93. (Previously presented) The method of any one of claims 81, 82 or 84, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with at least one reference level stored in at least one of the memory cells.

94. (Withdrawn) The method of any one of claims 81, 83 or 85, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with two or more reference levels stored in two or more of the memory cells.

95. (Previously presented) The method of claim 81, where resetting said blocks includes selecting said number of blocks less than all of the blocks in the array by electronically tagging said number of blocks, and then simultaneously applying reset voltage conditions to the memory cells within all of the selected blocks.

96. (Currently Amended) The method of any one of claims 81, 82 or 83, wherein the appropriate voltage conditions are applied to the plurality of memory cells within one of the reset

blocks in accordance with [[a]] said chunk of user data stored in a cache memory in response to additional space for new user data from a host being required in the cache memory.

97. (Previously presented) The method of claim 96, carried out on a single integrated circuit chip.

98. (Cancelled)

99. (Cancelled)

100. (Currently Amended) The method of any one of claims 81, 82 or 83, wherein the ~~memory~~ data storage system is enclosed in a card having a connector adapted to be ~~removeably~~ removably connected with a host system.